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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,674	03/18/2004	Anujan Varma	P18022	7998
46147	7590	08/02/2007		
RYDER IP LAW C/O INTELLEVATE P. O. BOX 52050 MINNEAPOLIS, MN 55402			EXAMINER ELPENORD, CANDAL	
			ART UNIT 2609	PAPER NUMBER
			MAIL DATE 08/02/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/804,674

Applicant(s)

VARMA, ANUJAN

Examiner

Candal Elpenord

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-36 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-35 is/are rejected.
- 7) ☒ Claim(s) 20 and 36 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 14 January 2005.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because the term "the disclosure" recited in line 1. Correction is required. See MPEP § 608.01(b).
2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Information Disclosure Statement

4. The information disclosure statement (IDS) submitted on 14 January 2005 was considered by the examiner.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. **Claims 1-36** are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims **1, 6, 12, 14, 31, 15-16** of copending Application No. 10/744199. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons:

For claims 1, 7, 12-16, 19, 27-30, 34, the claims **1, 12, 14, 31, 15-16** of copending Application No. 10/744199 discloses the switching device comprising:

- (a) a plurality of ingress ports to receive data from external sources;
- (b) a plurality of egress ports to transmit data to external destinations;

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(c) a plurality of queues to store data waiting to be transmitted from a particular ingress port to a particular egress port;

(d) a request generator to generate requests for permission to transmit data for the queues, wherein a request indicates a cumulative amount of data contained in a respective queue;

(e) a switching matrix to provide selective connectivity between the plurality of ingress ports and the plurality of egress ports; and

(f) a scheduler to receive the requests, generate grants based thereon, and configure the switching matrix, wherein said scheduler operates on a pipeline schedule and modifies the requests received to account for grants generated in current period or previous period that are not reflected in the queues yet as recited in **claim 1**, the device of **claim 12**, further comprising a framer to aggregate a plurality of segments to form a frame, wherein the frame has a maximum frame length, wherein the segments are retrieved from the at least one queue, and wherein the frame may contain segments associated with different packets as recited in **claim 14 (which corresponds to claim 1 of the instant application, claim 15-16 and 19)**; the device, further comprising a striper to stripe the data across a plurality of channels as recited in **claim 16 (which corresponds to claim 13 of the instant application)**; the device wherein the plurality of queues include at least one queue per priority as recited in **claim 6 (which corresponds to claim 7 of the instant application)**, a store and forward device a store and forward device comprising:

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(a) a plurality of Ethernet cards to receive data from and transmit data to external sources, wherein the plurality of Ethernet cards include

(b) an egress interface module to receive packets, store the packets as segments in queues associated with at least some subset of destination and priority, aggregate multiple segments to form frame, transmit the segments within the frame together, and generate requests for permission to transmit data from the queues, wherein the segments larger than a maximum segment size are divided into multiple segments, wherein the frames may include segments associated with different packets, and wherein the requests include external factors including at least some subset of quantity, priority and age; and

(c) an egress interface module to receive frames, divide the frames into segments, store the segments in a queue, monitor the queues for complete packets, and reassemble a packet after segments making up the packet are received;

(d) a switching matrix to provide connectivity between the Ethernet cards

(e) a backplane consisting of a plurality of channels to connect the plurality of Ethernet cards to the switching matrix; and

(f) a scheduler to receive the requests, assign the requests an internal priority based on the external factors, to configure the switching matrix accordingly, wherein the scheduler process the requests for the queues by internal priority in order to generate grants (**which corresponds to claim 27 and 34 of the instant application**) except aggregate multiple segments together to form a frame, transmit the segments within the frame together, the scheduler operating on a pipeline schedule, and modifying the

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requests received to account for grants generated in current period or previous period that are not reflected in the queues yet, the device, wherein the backplane is optical as recited in **claim 32 (which corresponds to claim 32 of the instant application)**, the device, wherein the switching matrix is optical as recited in **claim 33 (which corresponds to claim 32 of the instant application)**.

For claims 1, 7, 12-16, 19, 27-30, 34, the claims **1, 6, 12, 14, 31, 15-16** of copending Application No. 10/744199 disclose all the subject matter of the claimed invention with the exception of state monitor to track complete packets contained within the queue as recited in **claim 19** and **claim 27**, the apparatus, wherein the frames are striped over a plurality of channels and the receiver is a deskewer that receives the frame over the plurality of channels and deskews the stripes and combine them into the frame as recited in **claim 20** the device, wherein the backplane also connects the plurality of Ethernet cards to the scheduler as recited in **claim 28**, the device, wherein the backplane uses the same channels to connect the Ethernet cards to the switching matrix and to the scheduler as recited in **claim 29**, the device, wherein the backplane provides a logical separation of data path between the Ethernet cards and the switching matrix and scheduling path between the Ethernet and the scheduler as recited in **claim 30**, and the device, wherein the maximum frame size is selected based on at least some subset of configuration time of data paths, scheduling time for scheduler, and complexity of scheduling algorithms as recited in **claim 31**. However, monitoring the queues for complete packets, connecting the backplane to a plurality of Ethernet cards and the scheduler, the backplane using the same channels to connect to the switching

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matrix, to the scheduler and the Ethernet cards, the backplane providing a logical separation between of data path between the Ethernet cards, the switching matrix, the scheduler path, the device, wherein the maximum frame size is selected based on at least some subset of configuration time of data paths, scheduling time for scheduler, and complexity of scheduling algorithms, a deskewer being that stripes the frames over a plurality of channels are well known in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching methods as taught by the copending Application No. 10/744199 in order to produce the claimed invention of the instant application. The teaching methods as well the apparatus/device as taught by the copending Application No. 10/744199 can be modified for use into the teaching methods of the instant application by connecting the backplane, scheduler, and Ethernet cards to the crossbar or switching matrix where packets would be processed into frames. The motivation would be to provide bandwidth control of the switching device and service priority.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

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applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. **Claims 1-4 9-10, 13 and 15-18** are rejected under 35 U.S.C. 102(e) as being anticipated by **Antal et al. (US 7,224,703 B2)**.

As per claim 1, Antal et al. teaches the switching device comprising:

(a) a segmentation unit (**see fig. 4 box 22**) to receive data packets of variable size and to store the data packets as segments (**see column 8 line 4-7**) wherein the data packets received having a length greater than a maximum segment length are divided into multiple segments (**see column 3 line 6-9**);

(b) a plurality of queues to store the segments, wherein the queues are associated with destinations (**see column 8 line 4-7**);

(c) a scheduler (**see Fig. 9 box 62**) to generate a schedule including a data path from at least one queue to an associated destination (**see column 4 line 57-63**);

(d) a framer (**see Fig. 4 box 22 which is the framer**) to aggregate a plurality of segments to form a frame (**see Fig. 1 and 2 where the blocks indicate the block frames of different data packets, thus the segmenter is the framer**), wherein the frame has a maximum frame length, wherein the segments are retrieved from the at least one queue, and wherein the frame may contain segments associated with different data packets (**see column 4 line 64-67**); and

(e) a transmitter to transmit the frame to the associated destination, wherein the segments within the frame are transmitted together (**see abstract line 15-16**)

As per claim 2, Antal et al. discloses the device, wherein the segmentation unit divides the data packets having a length greater than the maximum segment length to form at least a first segment having the maximum segment length (**see column 3 line 36-42**).

As per claim 3, Antal et al. discloses the device, wherein a last segment formed by the segmentation unit may be less than the maximum segment length (**see column 2 line 15-17**).

As per claim 4, Antal et al. discloses the device, wherein the segmentation unit identifies a final segment belonging to a particular packet (**see column 1 line 62-68**).

As per claim 9, the device, wherein the framer forms the frames (**see column 4 line 57-50**) by aggregating complete segments.

As per claim 10, the device, wherein the framer pads the frame to reach the maximum frame length (**see column 8 line 23-28**).

As per claim 13, Antal et al. discloses the device, further comprising a striper to stripe the frame across a plurality of channels ((**see column 5 line 52-56**) **striping implies breaking data packets into block of segments/frames and then transmit the segment blocks over a communication medium**)).

Similarly, **claim 15** is rejected for the same reasons as claim 1 since it is the corresponding method of the device claim, so are **claim 17-18**, that are the corresponding method claims of the device claims 9 and 13.

As per claim 16, Antal et al. discloses the method, wherein the forming segments includes dividing the data packets having a length greater than the maximum

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segment length into at least a first segment having the maximum segment length (**see column 3 line 36-42**), and wherein a last segment formed may be less than the maximum segment size (**see column 2 line 15-17**).

Claims 27-31 and 34-35 are rejected under 35 U.S.C. 102(e) as being anticipated by **Muthukrishnan et al. (US 2005/0135355 A1)**.

As per claim 27, Muthukrishnan et al. discloses a store and forward device (**see paragraph 0019 line 1-3**) comprising:

(a) a plurality of Ethernet cards to receive data from and transmit data to external sources, wherein the plurality of Ethernet cards (**see paragraph 0022 line 3-5**) include

(b) an ingress interface module to receive packets of variable size, store the packets as segments in queues associated with at least some subset of destination (**see paragraph 0024 line 2-7**) and priority (**see paragraph 0028 line 1-5**), aggregate multiple segments together to form a frame, and transmit the segments within the frame together (**see paragraph 0029 line 1-7**), wherein the segments stored in the queues have a segment maximum size (**see paragraph 0026 line 9-11**) and the packets having a larger size are divide into multiple segments; and wherein the frames have a maximum frame size, include a plurality of segments and may include segments associated with different packets (**see paragraph 0026 line 11-12**), and

(c) an egress interface module to receive the frames, divide the frames into segments, store the segments in queue, monitor the queues for complete packets, and reassemble a packet after the segments making up the packet are received (**see paragraph 0024 line 2-7**);

(d) a switching matrix to provide selectivity between the Ethernet cards (**see paragraph 0041 line 5-7**);

(e) a backplane consisting of a plurality of channels to connect the plurality of Ethernet cards to the switching matrix (**see paragraph 0022 line 6-7**); and

(f) a scheduler to select connectivity between Ethernet cards and to configure the switching matrix (**see paragraph 0037 line 1-4**).

As per claim 28, Muthukrishnan et al. discloses the device, wherein the backplane also connects the plurality of Ethernet cards to the scheduler (**see paragraph 0044 line 5-7**).

As per claim 29, Muthukrishnan et al. discloses the device, wherein the backplane uses same channels to connect the Ethernet cards to the switching matrix and to the scheduler (**see paragraph 0044 line 3-8**).

As per claim 30, Muthukrishnan et al. discloses the device, wherein the backplane provides a logical separation of data path between the Ethernet cards and the switching matrix and scheduling path between the Ethernet cards and the scheduler (**see paragraph 0024 line 13-19**).

As per claim 31, Muthukrishnan et al. discloses the device, wherein the maximum frame size is selected based on at least some subset of configuration time of data path (**see paragraph 0030 line 6-9**), scheduling time for scheduler, and complexity of scheduling algorithms (**see paragraph 0033 line 1-5**).

As per claim 32, Muthukrishnan et al. discloses the device, wherein the backplane is optical (**see paragraph 0023 line 17**).

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As per claim 33, Muthukrishnan et al. discloses the device, wherein the switching matrix is optical (**see paragraph 0023 line 17**).

Claim 34 is rejected for the same reasons as claim 27.

As per claim 35, Muthukrishnan et al. discloses the device, wherein a pipeline schedule (**see paragraph 0046 line 1-2**) is implemented that includes at least some subset of:

(a) the ingress interface modules forming and transmitting requests to the scheduler (**see paragraph 0046 line 3-5**),

(b) scheduler computing a schedule based on the requests (**see paragraph 0046 line 5-7**), and

(c) the scheduler transmitting grants to associated ingress interface modules (**see paragraph 0046 line 9-12**) and configuring the switching matrix (**paragraph 0046 line 13-14**),

(d) the ingress interface modules transmitting the frames in response to the grants (**paragraph 0046 line 19-20**).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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10. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. **Claims 5-7** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Antal et al.** in view of **Dell et al. (US 7,023,841 B2)**.

As per claims 5-7, Antal et al. teaches all the subject matter of the claimed invention with the exception of the device wherein the scheduler generates the schedule based on requests for data packets from particular queues to be transmitted to particular destinations as recited in **claim 5**, the device wherein the scheduler matches the requests and resolves conflicts in order to generate the schedule as recited in **claim 6**, the device, wherein the plurality of queues include one or more queues per destination based on priorities associated with the destinations as recited in **claim 7**. However, **Dell et al.** in a similar field of endeavor teaches the device wherein the scheduler generates the schedule based on requests for data packets from particular queues to be transmitted to particular destinations (**see column 3 line 28-34**) as recited in **claim 5**, the device wherein the scheduler matches the requests and resolves conflicts in order to generate the schedule (**see column 3 line 35-42**) as recited in **claim 6**, and the device, wherein the plurality of queues include one or more queues per destination based on priorities associated with the destinations (**see column 13 line 39-**

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46) as recited in **claim 7**. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was to incorporate the switching fabric apparatus as taught by **Dell et al.** into the segmentation apparatus of **Antal et al.** in order to do schedule arbitration between multiple requests for transmission by different ports and service priority queuing. The switching apparatus as taught by **Dell et al.** can be modified for use into the segmentation apparatus of **Antal et al.** by connecting the segmentation device to the switching apparatus. Additionally, this can be accomplished through software and hardware manipulation. The motivation would be to provide efficient sharing of the switching device bandwidth.

Claims 8, and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Antal et al.** in view of **Davidson et al.**

As per **claims 8, and 11-12**, **Antal et al.** teaches all the subject matter of the claimed invention of explicitly disclosing the device, wherein the framer forms the frame by aggregating segments from some subset of the one or more associated queues as recited in **claim 8**, the device, wherein the transmitter transmits the segments making up a particular data packet in order as recited in **claim 11**, the device, wherein the transmitter interleaves segments associated with different data packets as recited in **claim 12**. However, **Davidson et al.** in a similar field of endeavor teaches the device wherein the framer (see **Fig. 1 box 20**) forms the frame by aggregating segments from some subset of the one or more associated queues (see **column 1-2 line 1-5**) as recited in **claim 8**, the device, wherein the transmitter transmits the segments making up a particular packet in order (see **column 3 line 8-10**) as recited in **claim 11**, the device,

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wherein the transmitter interleaves segments associated with many different data packets (**see column 2 line 42-50**) as recited in **claim 12**. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the method and apparatus of aggregating data blocks within a network processor into the teaching methods of **Antal et al.** so that the data blocks of frames can be reassembled. The method and apparatus of reassembling of data blocks from the segments as taught by **Davidson et al.** can be modified/implemented for use into the teaching methods of **Antal et al.** through a network-processing device by attaching an indicator to each packet block. The motivation would be for transmission integrity of data blocks in the queue.

12. **Claim 14** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Antal et al.** in view of background of **Muthukrishnan al. (US 2005/0135356 A1)**.

As per claim 14, Antal et al. teaches all the subject matter of the claimed invention with the exception of the device, further comprising a switch fabric to provide a configurable connection between a plurality of sources and a plurality of destinations, wherein the switch fabric is configured by the scheduler, and wherein the switch fabric transmits frames from at least a subset of the plurality of sources to at least a subset of the plurality of destinations during a schedule cycle as recited in **claim 14**. However, **Muthukrishnan al. ("356")**, in his background of his invention discloses the device, further comprising a switch fabric to provide a configurable connection between a plurality of sources and a plurality of destinations (**see background paragraph 0001**

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line 8-14) wherein the switch fabric is configured by the scheduler (**see background paragraph 0002 line 1-5**), and wherein the switch fabric transmits frames from at least a subset of the plurality of sources to at least a subset of the plurality of destinations during a schedule cycle (**see background paragraph 0003 line 11-18**). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the background teaching disclosure as shown by **Muthukrishnan et al.** into the teaching methods of **Antal et al.** so that transmission of frames can be synchronized. The prior art disclosed in background of **Muthukrishnan et al.** can be modified to include the teaching methods of **Antal et al.** through network processor. The motivation would be for reducing transmission delays associated with frames processing.

14. **Claim 19, 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davidson et al. in view of background of Muthukrishnan et al. (US 2005/0135356 A1).**

As per claims 19, 21 and 23, Davidson et al. discloses the apparatus comprising:

(a) a plurality of sources; a plurality of destinations (**see Fig. 4 box 12 and box 14**);

(b) a receiver to receive frames, wherein the frames include a plurality of segments and the segments may be associated with multiple data packets (**see column 2 line 42-50**);

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- (c) a deframer to extract the segments from the frame (**see column 3 line 2-5**);
- (d) a queue to store the segments (**see Fig. 1 box 26 and column 3 line 20-23**);
- (e) a state monitor to track complete packets contained within the queue (**see column 3 line 53-55**);
- (f) a reassembly unit (**see box 14 of fig. 1**) to combine the segments making up a complete packet together to generate the packets (**see column 2 line 34-41**);

As per claim 21, Davidson et al. teaches the apparatus, further comprising an error checker to for errors in the frame (**see column 3 line 11-12**).

As per claim 23, Davidson et al. teaches the apparatus, wherein the state monitor determines complete packets by detecting an end of packet (**see column 3 line 27-30**). **Davidson et al.** teaches all the subject matter of the claimed invention with the exception of a scheduler to generate a schedule for transmitting frames; and a switch fabric to selectively connect the plurality of sources to the plurality of destinations based on the schedule, wherein the switch fabric transmits frames from at least a subset of the plurality of sources to at least a subset of the plurality of destinations as recited in **claim 19**. However, **Muthukrishnan et al. ('356')**, in a similar field of endeavor discloses in his background a scheduler to generate a schedule for transmitting frames (**see background paragraph 0003 line 11-13**); and a switch fabric to selectively connect the plurality of sources to the plurality of destinations based on the schedule (**see background paragraph 0001 line 8-14**), wherein the switch fabric transmits frames (**see background paragraph 0003 line 3-7**) from at least a subset of the plurality of sources to at least a subset of the plurality of destinations. Therefore, it would have

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been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the method/ apparatus of data block as taught by **Davidson et al.** into the disclosure of background of **Muthukrishnan et al.** in order to compute schedule for the segments (frames). The method/ apparatus of data block as taught by **Davidson et al.** can modified/implemented for use into the background disclosure of **Muthukrishnan et al.** by connecting the scheduler along with the switching fabric to the apparatus disclosed by **Davidson et al.** The motivation would be to provide fast processing of segments (frames).

Claims 24-26 are rejected for the same reasons as claim 19, 21 and 23 since they are the corresponding method claims of the apparatus claims.

13. **Claim 22** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Davidson et al.** in view of background disclosure **Muthukrishnan et al.** in further view of **Muthukrishnan et al. (US 2005/0135355 A1)**.

For claim 22, **Davidson et al.** and background disclosure of **Muthukrishnan et al. ('356')** disclose all the subject matter of the claimed invention with the exception of the apparatus, wherein the error checker checks for errors by comparing a grant received to the frame. However, **Muthukrishnan et al. ('355')** in a similar field of endeavor discloses the apparatus, wherein the error checker checks for errors by comparing a grant received to the frame (see paragraph 0080 line 1-7). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching methods and apparatus as taught by **Muthukrishnan et al. ('355')** into the teaching methods as disclosed by **Davidson et al.** and background

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disclosure of **Muthukrishnan et al. ('356')** in order to determine error in the frames.

The error checker apparatus as taught by **Muthukrishnan et al.** can be modified for use into the teaching methods as disclosed by **Davidson et al.** and background disclosure of **Muthukrishnan et al. ('356')** by connecting the frame error checker to an interface module. The motivation would be for maintaining frame integrity.

Allowable Subject Matter

15. **Claim 20 and 36** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. May et al. (US 2004/0252688 A1), Yamamoto et al. (US 6,993,041 B2), Colmant et al. (US 2006/0251124 A1), Hall et al. (US 2006/0165070 A1) and Bansal et al. (US 7,246,303 B2) are cited to method and systems related to the claimed invention.

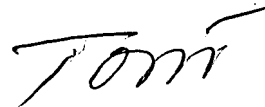
17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Candal Elpenord whose telephone number is (571) 270-3123. The examiner can normally be reached on Monday through Friday 7:30AM to 5:00PM EST.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dang Ton can be reached on (571) 272-3171. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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CE

A handwritten signature in black ink, appearing to read 'Dang T. Ton' in a cursive style.

DANG T. TON
SUPERVISORY PATENT EXAMINER